AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method for creating a mask-programmable module from standard cells, comprising:

specifying characteristics of an end design;

selecting a plurality of standard cells from a standard cell library based on the characteristics of the end design;

combining the plurality of standard cells into a mask-programmable module, wherein instances of the mask-programmable module are repeated to form a mask-programmable fabric; and

designing a mask-programmable interconnect to match the mask-programmable module, whereby connections within the mask-programmable module and between mask-programmable modules are ~~can be~~ generated by programming the mask-programmable interconnect.

2. (Currently amended) The method of claim 1, wherein the mask-programmable modules and the mask-programmable interconnect that make up the mask-programmable fabric are ~~can be~~ programmed by changing inter-metal via layers and/or metal layers.

3. (Original) The method of claim 1, wherein combining the plurality of standard cells into a mask-programmable module additionally involves defining connections between standards cells within the mask-programmable module.

4. (Currently amended) The method of claim 1, further comprising generating views for the mask-programmable module, wherein the views ~~can~~ include:

a physical view that specifies connectivity within the mask-programmable module, including connectively with pins in the mask-programmable module;

a logical view that specifies logical relationships between signals in the mask-programmable module; and

a timing view that specifies timing relationships within the mask-programmable module.

5. (Original) The method of claim 4, wherein generating the views involves using pre-existing information about the plurality of the standard cells from the standard cell library to generate the views for the mask-programmable module.

6. (Original) The method of claim 1, further comprising:

receiving a high-level design for an integrated circuit; and

performing a synthesis operation on the high-level design to generate a netlist for the high-level design that contains references to mask-programmable modules.

7. (Original) The method of claim 6, further comprising performing a placement operation and a routing operation on the netlist to produce a layout for the integrated circuit.

8. (Original) The method of claim 7, wherein performing the routing operation involves programming the mask-programmable modules and mask-programmable interconnect.

9. (Currently amended) A computer-readable storage medium storing instructions that when executed by a computer cause the computer to perform a method for creating a mask-programmable module from standard cells, the method comprising:

specifying characteristics of an end design;

selecting a plurality of standard cells from a standard cell library based on the characteristics of the end design;

combining the plurality of standard cells into a mask-programmable module, wherein instances of the mask-programmable module are repeated to form a mask-programmable fabric; and

designing a mask-programmable interconnect to match the mask-programmable module, whereby connections within the mask-programmable module and between mask-programmable modules are ~~can be~~ generated by programming the mask-programmable interconnect.

10. (Currently amended) The computer-readable storage medium of claim 9, wherein the mask-programmable modules and the mask-programmable interconnect that make up the mask-programmable fabric are ~~can be~~ programmed by changing inter-metal via layers and/or metal layers.

11. (Original) The computer-readable storage medium of claim 9, wherein combining the plurality of standard cells into a mask-programmable module additionally involves defining connections between standards cells within the mask-programmable module.

12. (Currently amended) The computer-readable storage medium of claim 9, wherein the method further comprises ~~comprising~~ generating views for the mask-programmable module, wherein the views ~~can~~ include:

a physical view that specifies connectivity within the mask-programmable module, including connectively with pins in the mask-programmable module;

a logical view that specifies logical relationships between signals in the mask-programmable module; and

a timing view that specifies timing relationships within the mask-programmable module.

13. (Original) The computer-readable storage medium of claim 12, wherein generating the views involves using pre-existing information about the plurality of the standard cells from the standard cell library to generate the views for the mask-programmable module.

14. (Currently amended) The computer-readable storage medium of claim 9, wherein the method further comprises ~~comprising~~:

receiving a high-level design for an integrated circuit; and

performing a synthesis operation on the high-level design to generate a netlist for the high-level design that contains references to mask-programmable modules.

15. (Currently amended) The computer-readable storage medium of claim 14, wherein the method further comprises ~~comprising~~ performing a placement operation and a routing operation on the netlist to produce a layout for the integrated circuit.

16. (Original) The computer-readable storage medium of claim 15, wherein performing the routing operation involves programming the mask-programmable modules and mask-programmable interconnect.

17. (Currently amended) An apparatus for creating a mask-programmable module from standard cells, comprising:

a specifying mechanism configured to specify characteristics of an end design;

a selecting mechanism configured to select a plurality of standard cells from a standard cell library based on the characteristics of the end design;

a combining mechanism configured to combine the plurality of standard cells into a mask-programmable module, wherein instances of the mask-programmable module are repeated to form a mask-programmable fabric; and

a designing mechanism configured to design a mask-programmable interconnect to match the mask-programmable module, whereby connections within the mask-programmable module and between mask-programmable modules are ~~can be~~ generated by programming the mask-programmable interconnect

18. (Currently amended) The apparatus of claim 17, wherein functions of the mask-programmable modules and the mask-programmable interconnect that make up the mask-programmable fabric are ~~can be~~ programmed by changing inter-metal via layers and/or metal layers.

19. (Original) The apparatus of claim 17, wherein combining the plurality of standard cells into a mask-programmable module additionally involves defining connections between standards cells within the mask-programmable module.

20. (Currently amended) The apparatus of claim 17, further comprising a generating mechanism configured to generate views for the mask-programmable module, wherein the views ~~can~~ include:

a physical view that specifies connectivity within the mask-programmable module, including connectively with pins in the mask-programmable module;

a logical view that specifies logical relationships between signals in the mask-programmable module; and

a timing view that specifies timing relationships within the mask-programmable module.

21. (Original) The apparatus of claim 20, wherein generating the views involves using pre-existing information about the plurality of the standard cells from the standard cell library to generate the views for the mask-programmable module.

22. (Original) The apparatus of claim 17, further comprising:

a receiving mechanism configured to receive a high-level design for an integrated circuit; and

a synthesis mechanism configured to perform a synthesis operation on the high-level design to generate a netlist for the high-level design that contains references to mask-programmable modules.

23. (Original) The apparatus of claim 22, further comprising a place-and-route mechanism configured to perform a placement operation and a routing operation on the netlist to produce a layout for the integrated circuit.

24. (Original) The apparatus of claim 23, wherein performing the routing operation involves programming the mask-programmable modules and mask-programmable interconnect.